

<b>FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE (Modified) PATENT AND TRADEMARK OFFICE</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use several sheets if necessary)	<b>ATTY. DOCKET NO.</b> <b>59165-298553</b>	<b>APPLN. NO.</b> 10/717 386 <b>Not yet known</b>
	<b>APPLICANT:</b> <b>NARAIN et al.</b>	
	<b>FILING DATE</b> <b>Herewith 11/18/03</b>	<b>GROUP</b> 2825 <b>Not yet known</b>

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
VS	5,517,432	05-14-1996	Chandra et al.	364	578.1	
	5,604,895	02-18-1997	Raimi	395	500	
	5,680,332	10-21-1997	Raimi et al.	364	578	
	5,774,370	06-30-1998	Giomi	716	4	
	<del>6,175,946</del>	<del>01-16-2001</del>	<del>Ly et al.</del>	<del>716</del>	<del>4</del>	<del>Dup.</del>
VS	6,182,268	01-30-2001	McElvain	716	1	

## FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	DOCUMENT NUMBER	PUBLISHED DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
VS	PCT/US01/14973	03-11-02	Europe				

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

VS	Chang et al., "Verification of a Microprocessor Using Real World Applications," IEEE, (June 1999), pp. 181-184.
	Goldberg et al. "Combinational Verification Based on High-Level Functional Specifications," IEEE, (January 1998), pp. 1-6.
	Eijk et al., "Exploiting Functional Dependencies in Finite State Machine Verification," IEEE, (1996), pp. 9-14.
	York et al., "An Integrated Environment for HDL Verification," IEEE, (1995), pp. 9-18.
	Switzer, et al., "Functional Verification with Embedded Checkers," 3 pages.
	Switzer, et al., "Functional Verification with Embedded Checkers," 5 pages.
	"0-In Ships Industry's First White-Box Verification Tool," 0-In Design Automation, Inc.
	Chandra et al., "Architectural Verification of Processors Using Symbolic Instruction Graphs," Proceedings, IEEE International Conference on Computer Design: VLSI in Computers and Processors, Cambridge, Massachusetts, (October 10-12, 1994).
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4/06/06

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

US	Levitt, et al., "A Scalable Formal Verification Methodology for Pipelined Microprocessors," Proceedings 1996 33 <sup>rd</sup> Design Automation Conference, Las Vegas, Nevada, (1996).
	Moundanos, et al., "Abstraction Techniques for Validation Coverage Analysis and Test Generation," IEEE Transactions on Computers, Vol. 47, No. 1, (January 1998).
	Jones et al., "Self-Consistency Checking," International Conference on Formal Methods in Computer-Aided Design (PMCAD), (1996).
	Naik et al., "Modeling and Verification of a Real Life Protocol Using Symbolic Model Checking."
	Eiriksson et al., "Integrating Formal Verification Methods with a Conventional Project Design Flow," Proceedings of the 33 <sup>rd</sup> Design Automation Conference, Las Vegas, Nevada, (1996).
	Beer et al., "Methodology and System for Practical Formal Verification of Reactive Hardware," 6 <sup>th</sup> International Conference, CAV '94, (June 21-23, 1994).
	Balarin, "Formal Verification of Embedded Systems Based on CFSM Networks," Proceedings of the 33 <sup>rd</sup> Design Automation Conference, Las Vegas, Nevada, (1996).
	Ho, Chain-Min Richard, "Validation Tools for Complex Digital Designs," Department of Computer Science and the committee on Graduate Studies of Stanford University in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy, (November 1996).
	Burch et al., "Automatic Verification of Pipelined Microprocessor Control," Conference on Computer-Aided Verification, (June 21-23, 1994).
	Hoskote et al., "Automatic Extraction of the Control Flow Machine and Application to Evaluating Coverage of Verification Vectors," International Conference on Computer Design: VLS in Computers & Processors, (October 2-4, 1995).
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	Brand et al., "Incremental Synthesis," (1994), pp. 14-18.
	"Time Rover: The Formal Testing Company," (November 17, 1997), p. 1.
	"Solidification: Static Functional Verification with Solidify," (1999), pp. 1-10.
	"Solidify: Static Functional Verification for HDL Designers," (March 1999), 2 pages.
	"New Cadence Verification Product and Methodology Services Deliver Breakthrough Productivity for SOC Verification," Downloaded from <a href="http://www.cadence.com/press_box/na/pr/1999/06_07_99.html">http://www.cadence.com/press_box/na/pr/1999/06_07_99.html</a> on June 1999, pp. 1-3.
	"Formalized Design," Downloaded from <a href="http://www.formalized.com/prod.html/default_productspecman.html">http://www.formalized.com/prod.html/default_productspecman.html</a> on June 1999, p. 1.
	"Specman Elite Data Sheet," Downloaded from <a href="http://www.versity.com/html/default_productspecman.html">http://www.versity.com/html/default_productspecman.html</a> on July 1999, pp. 1-2.
	"0-In Methodology Overview," Downloaded from <a href="http://www.0-in.com/subpages/prodtech/index.html">http://www.0-in.com/subpages/prodtech/index.html</a> on July 1999, pp. 1-2.
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US	"Datasheet Affirma FormalCheck model checker," 1 page.

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## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

1/5		"Datasheet Affirma Coverage Analyzer," 1 page.
		"SureThing" the Designer's Workbench," 2 pages.
		"Twister: Automatic Model Checker Formal Verification of Designs Using Predefined Rules," 2 pages.
		"0-In Search Data Sheet," pp. 1-3.
		"0-In CheckerWare Data Sheet," pp. 1-2.
		"0-In Checker Data Sheet," pp. 1-3.
		"0-In Design Automation Home Page," Downloaded from <a href="http://www.0-in.com">http://www.0-in.com</a> on May 8, 2000, p. 1.
		"0-In Methodology Overview," Downloaded from <a href="http://www.0-in.com/subpages/prodtech/index.html">http://www.0-in.com/subpages/prodtech/index.html</a> on May 8, 2000, 2 pages.
		"0-In Check," Downloaded from <a href="http://www.0-in.com/subpages/prodtech/0in_check.html">http://www.0-in.com/subpages/prodtech/0in_check.html</a> on May 8, 2000, 2 pages.
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		Anderson, T., "Using VCS with White-Box Verification Techniques," SNUG, San Jose, (2000), pp. 1-9.
		Switzer et al., "Using Embedded Checkers to Solve Verification Challenges," pp. 1-20.
		Goering, Richard, "Verification Start-Up Seeks Design Intent," EE Times, (April 24, 2000), 2 pages.
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PTO/SB/08b (05-03)

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Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet 1 of 1

**Complete if Known**

Application Number	10/717,386
Filing Date	November 18, 2003
First Named Inventor	Prakash Narain et al.
Art Unit	2825
Examiner Name	Not yet known SIEK, V.
Attorney Docket Number	59165-298553

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
lt		SFORZA et al., "A 'Design for Verification' Methodology." March 2001. Quality Electronic Design. 2001 International Symposium. pp 50-55.	
vs		OMNES et al., "Using SSDE for USB2.0 Conformance Co-Verification." June 2003. Formal Methods and Models for Co-Design, 2003. MEMOCODE '03. Proceedings. First ACM and IEEE International Conference. pp. 113-122.	
lt		BHASKAR et al., "A Universal Random Test Generator for Functional Verification of Microprocessors and System-On-Chip." January 2005. VLSI Design 2005. 18 <sup>th</sup> International Conference. pp. 207-212.	

Examiner Signature	VUTHE SIEK	Date Considered	4/06/06
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1 citation designation number (optional). 2 See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

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